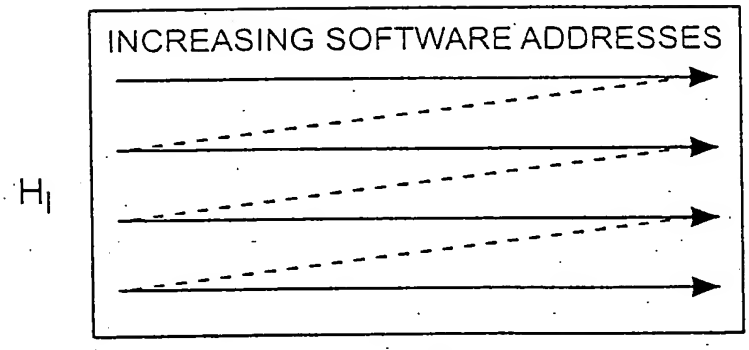

FIG._1a

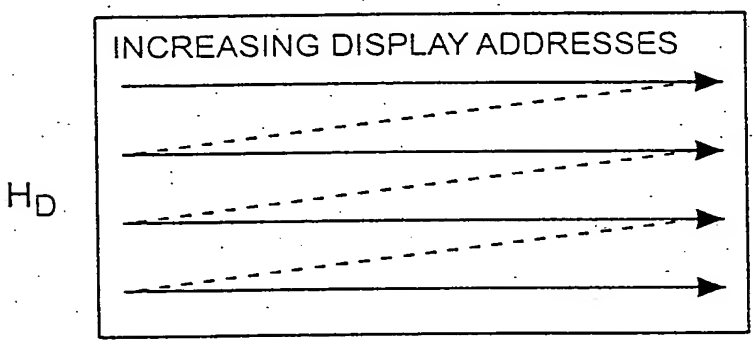

FIG._1b

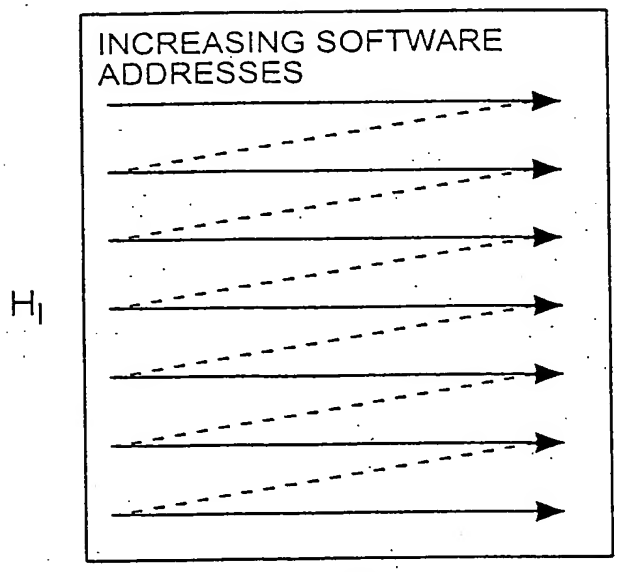

FIG._2a

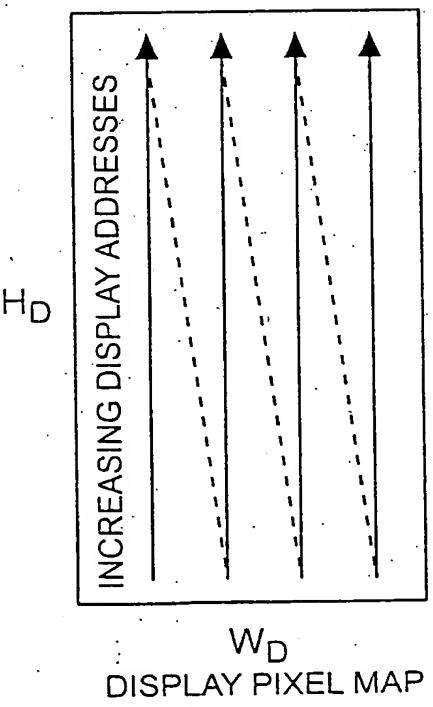

FIG._2b

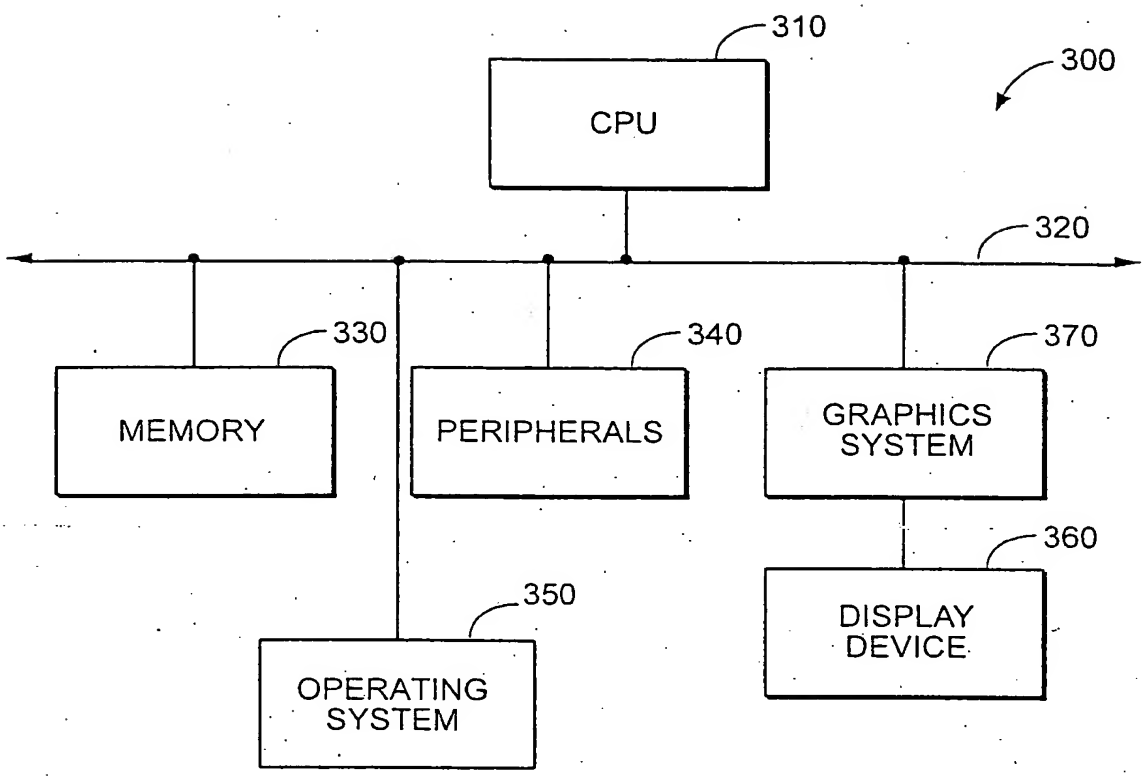
310
300
CPU
320
330
340
370
MEMORY
PERIPHERALS
GRAPHICS SYSTEM
360
350
DISPLAY DEVICE
OPERATING SYSTEM

FIG._3

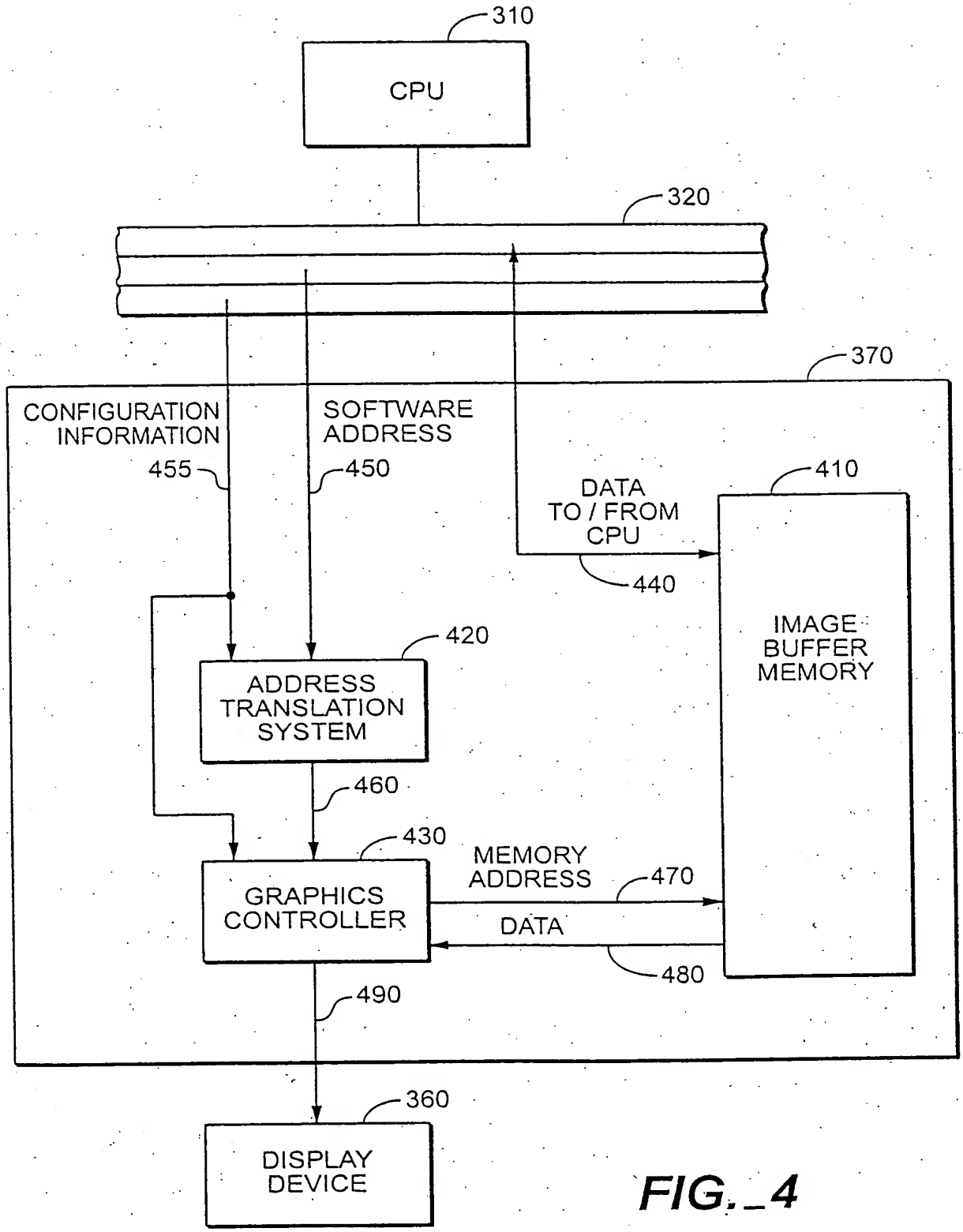
310
CPU
320
370
CONFIGURATION INFORMATION
SOFTWARE ADDRESS
455
450
DATA TO / FROM CPU
410
440
IMAGE BUFFER MEMORY
420
ADDRESS TRANSLATION SYSTEM
460
430
MEMORY ADDRESS
470
GRAPHICS CONTROLLER
DATA
480
490
360
DISPLAY DEVICE

FIG._4

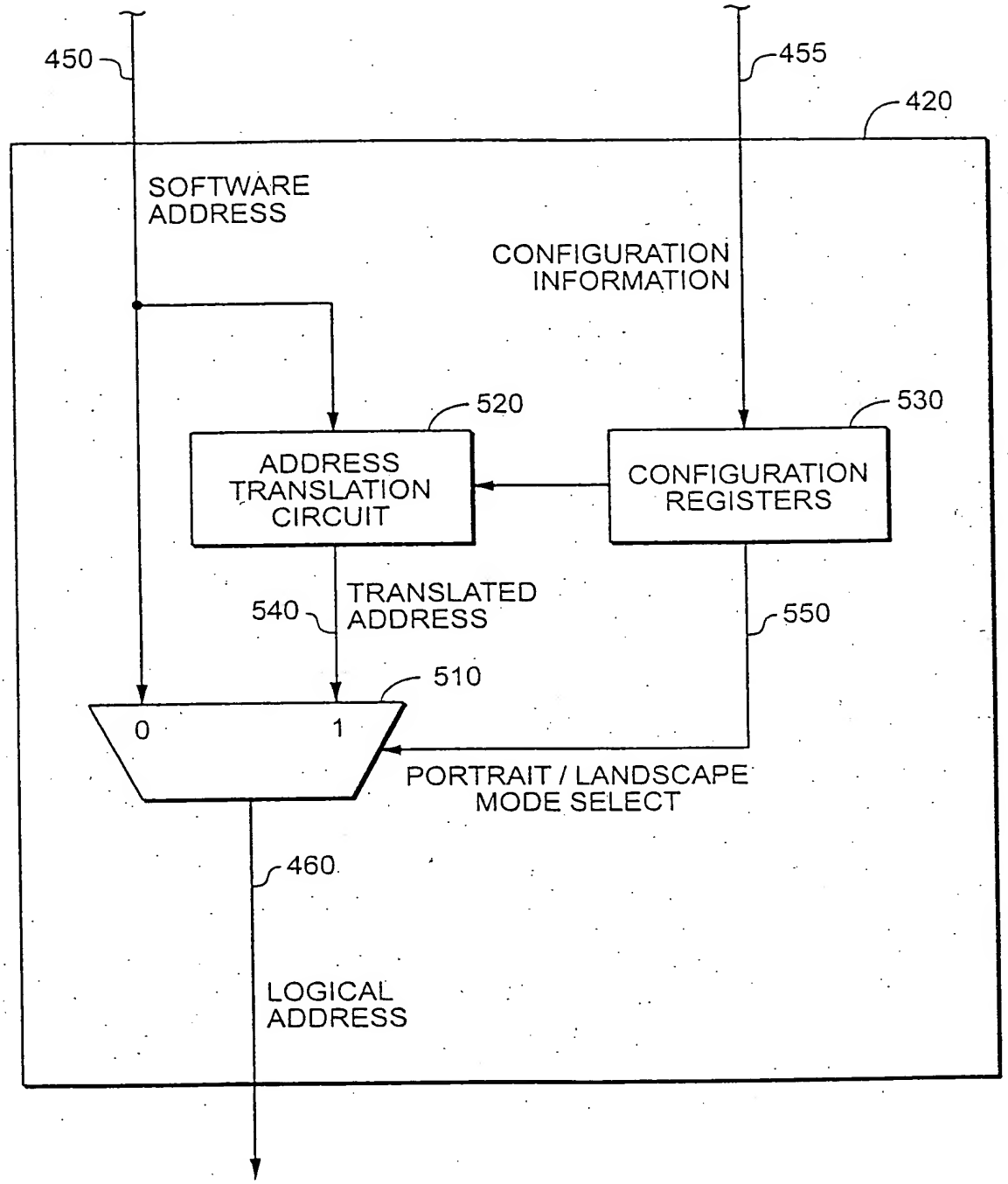
450
455
420
SOFTWARE ADDRESS
CONFIGURATION INFORMATION
520
530
ADDRESS TRANSLATION CIRCUIT
CONFIGURATION REGISTERS
540
TRANSLATED ADDRESS
550
510
0
1
PORTRAIT / LANDSCAPE MODE SELECT
460
LOGICAL ADDRESS

FIG._5

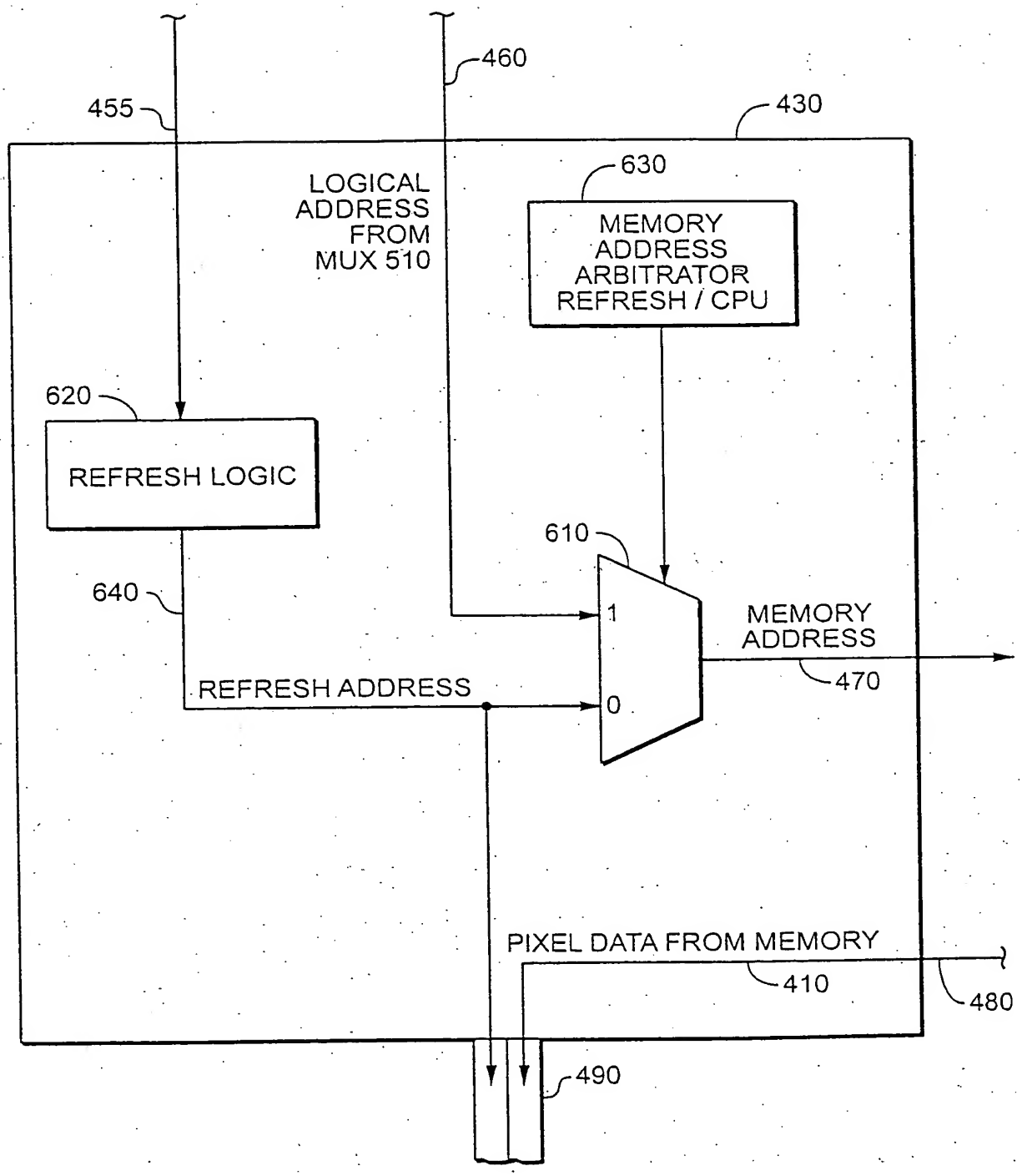
460
455
430
LOGICAL ADDRESS FROM MUX 510
630
MEMORY ADDRESS ARBITRATOR REFRESH / CPU
620
REFRESH LOGIC
610
640
1
MEMORY ADDRESS
470
REFRESH ADDRESS
0
PIXEL DATA FROM MEMORY
410
480
490

FIG._6

0	1	2	3	4	5	6	7
8	9	10	11	12	13	14	15
16	17	18	19	20	21	22	23
24	25	26	27	28	29	30	31

FIG._7a

7	15	23	31
6	14	22	30
5	13	21	29
4	12	20	28
3	11	19	27
2	10	18	26
1	9	17	25
0	8	16	24

FIG._7b

0	1	2	3
4	5	6	7
8	9	10	11
12	13	14	15
16	17	18	19
20	21	22	23
24	25	26	27
28	29	30	31

FIG._7d

0	0	1	1	1	0	1	1	1	1	1	0	1	1	1	1	1	1	1	1
0	0	1	1	0	0	1	1	1	0	1	0	1	1	0	1	1	1	1	0
0	0	1	0	1	0	1	1	0	1	1	0	1	0	1	1	1	1	0	1
0	0	1	0	0	0	1	1	0	0	1	0	1	0	0	1	1	1	0	0
0	0	0	1	1	0	1	0	1	1	1	0	0	1	1	1	1	0	1	1
0	0	0	1	0	0	1	0	1	0	1	0	0	1	0	1	1	0	1	0
0	0	0	0	1	0	1	0	0	1	1	0	0	0	1	1	1	0	0	1
0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	1	1	0	0	0

FIG._7c

LOGICAL ADDRESS	PHYSICAL ADDRESS	LOGICAL ADDRESS	PHYSICAL ADDRESS
0	0 0 1 1 1	16	0 0 0 1 1
1	0 1 1 1 1	17	0 1 0 1 1
2	1 0 1 1 1	18	1 0 0 1 1
3	1 1 1 1 1	19	1 1 0 1 1
4	0 0 1 1 0	20	0 0 0 1 0
5	0 1 1 1 0	21	0 1 0 1 0
6	1 0 1 1 0	22	1 0 0 1 0
7	1 1 1 1 0	23	1 1 0 1 0
8	0 0 1 0 1	24	0 0 0 0 1
9	0 1 1 0 1	25	0 1 0 0 1
10	1 0 1 0 1	26	1 0 0 0 1
11	1 1 1 0 1	27	1 1 0 0 1
12	0 0 1 0 0	28	0 0 0 0 0
13	0 1 1 0 0	29	0 1 0 0 0
14	1 0 1 0 0	30	1 0 0 0 0
15	1 1 1 0 0	31	1 1 0 0 0

A_1 A_0 $\overline{A_4}$ $\overline{A_3}$ $\overline{A_2}$ A_1 A_0 $\overline{A_4}$ $\overline{A_3}$ $\overline{A_2}$

FIG._7e

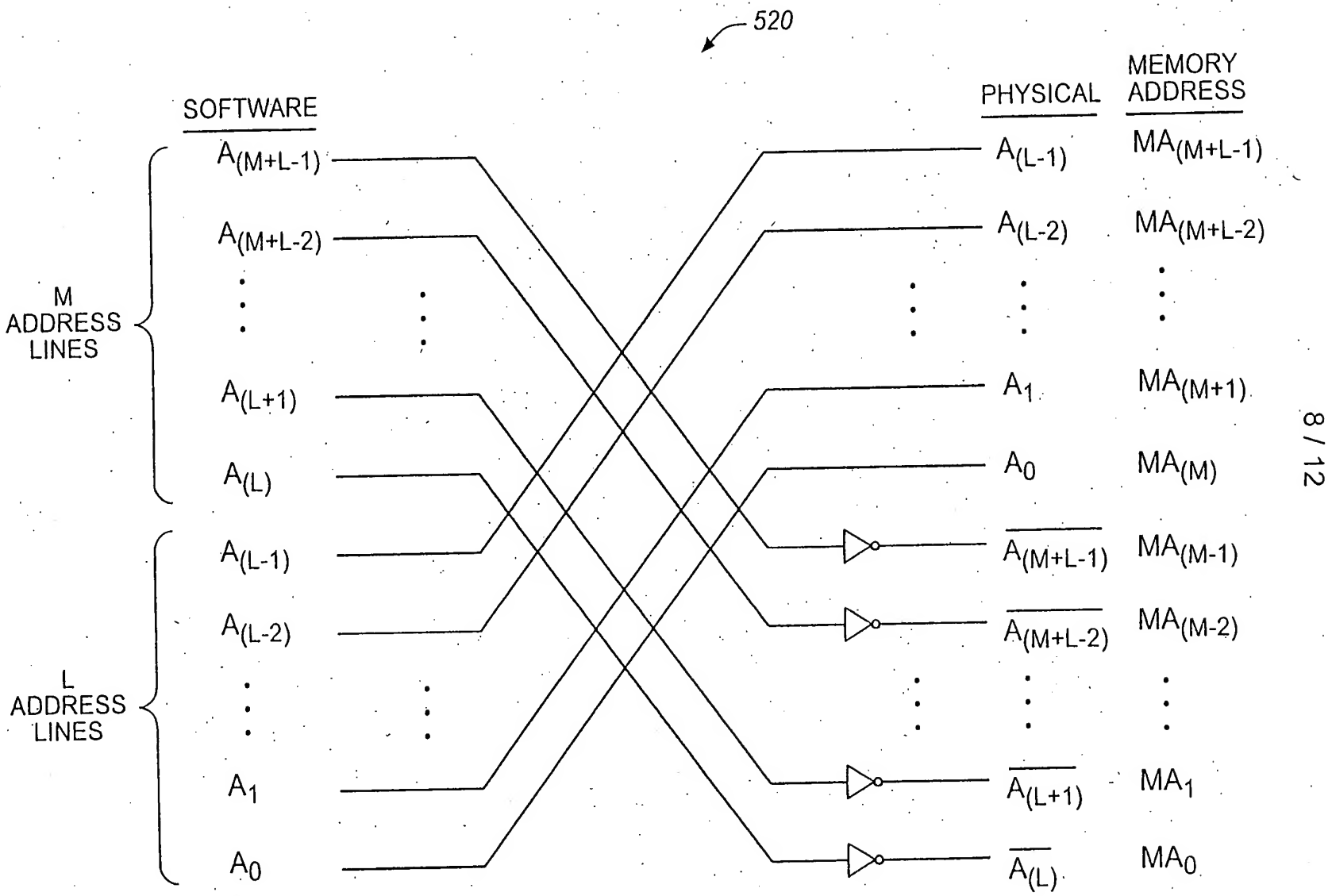
520
SOFTWARE
PHYSICAL
MEMORY ADDRESS
M ADDRESS LINES
L ADDRESS LINES
A(M+L-1)
A(M+L-2)
A(L+1)
A(L)
A(L-1)
A(L-2)
A1
A0
A(L-1)
A(L-2)
A1
A0
A(M+L-1)
A(M+L-2)
A(L+1)
A(L)
MA(M+L-1)
MA(M+L-2)
MA(M+1)
MA(M)
MA(M-1)
MA(M-2)
MA1
MA0

FIG._8

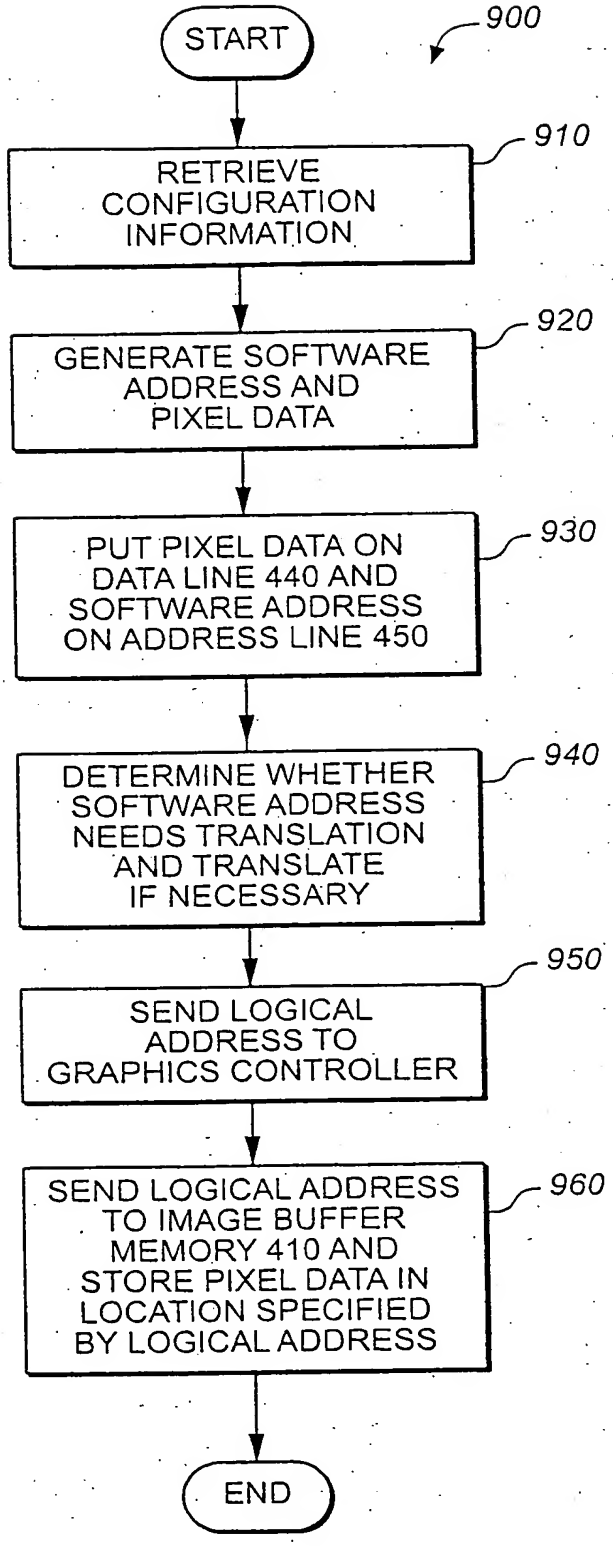
START
900
RETRIEVE CONFIGURATION INFORMATION
910
GENERATE SOFTWARE ADDRESS AND PIXEL DATA
920
PUT PIXEL DATA ON DATA LINE 440 AND SOFTWARE ADDRESS ON ADDRESS LINE 450
930
DETERMINE WHETHER SOFTWARE ADDRESS NEEDS TRANSLATION AND TRANSLATE IF NECESSARY
940
SEND LOGICAL ADDRESS TO GRAPHICS CONTROLLER
950
SEND LOGICAL ADDRESS TO IMAGE BUFFER MEMORY 410 AND STORE PIXEL DATA IN LOCATION SPECIFIED BY LOGICAL ADDRESS
960
END

FIG._9

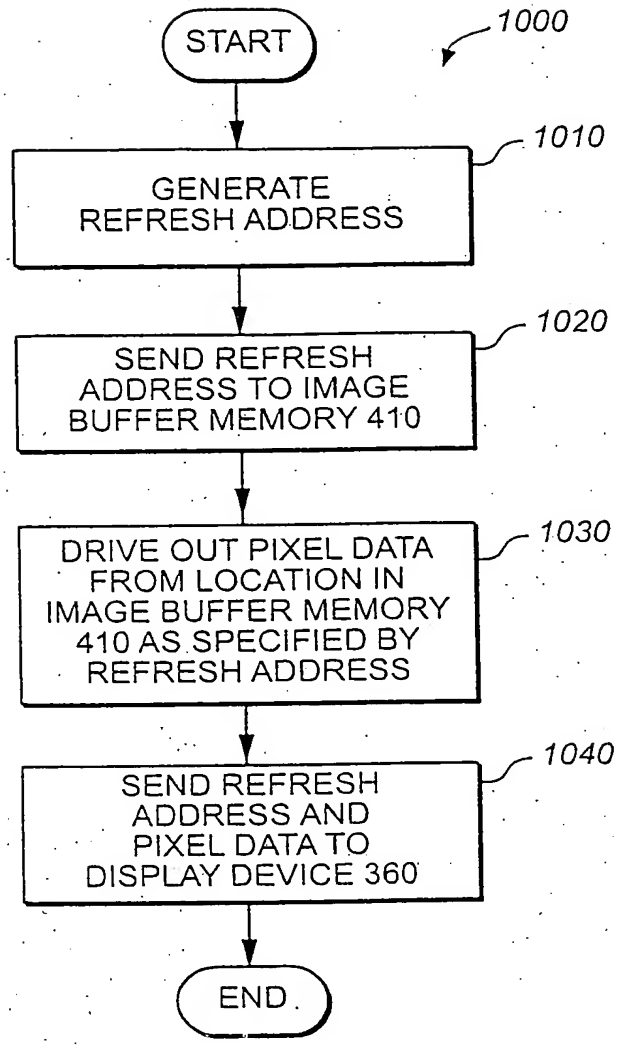
START
1000
GENERATE REFRESH ADDRESS
1010
SEND REFRESH ADDRESS TO IMAGE BUFFER MEMORY 410
1020
DRIVE OUT PIXEL DATA FROM LOCATION IN IMAGE BUFFER MEMORY 410 AS SPECIFIED BY REFRESH ADDRESS
1030
SEND REFRESH ADDRESS AND PIXEL DATA TO DISPLAY DEVICE 360
1040
END

FIG._10

BEST AVAILABLE COPY

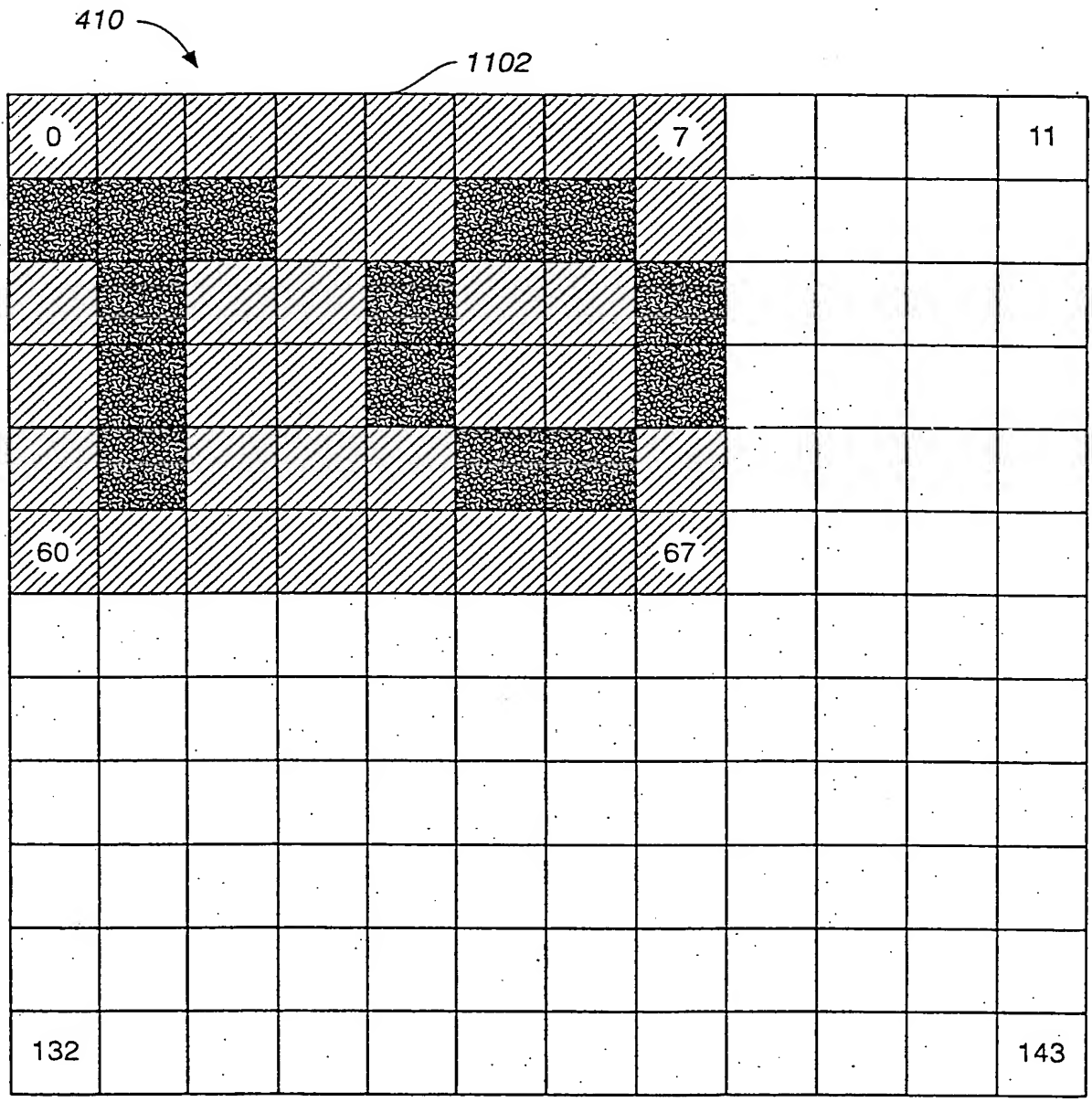

FIG._11

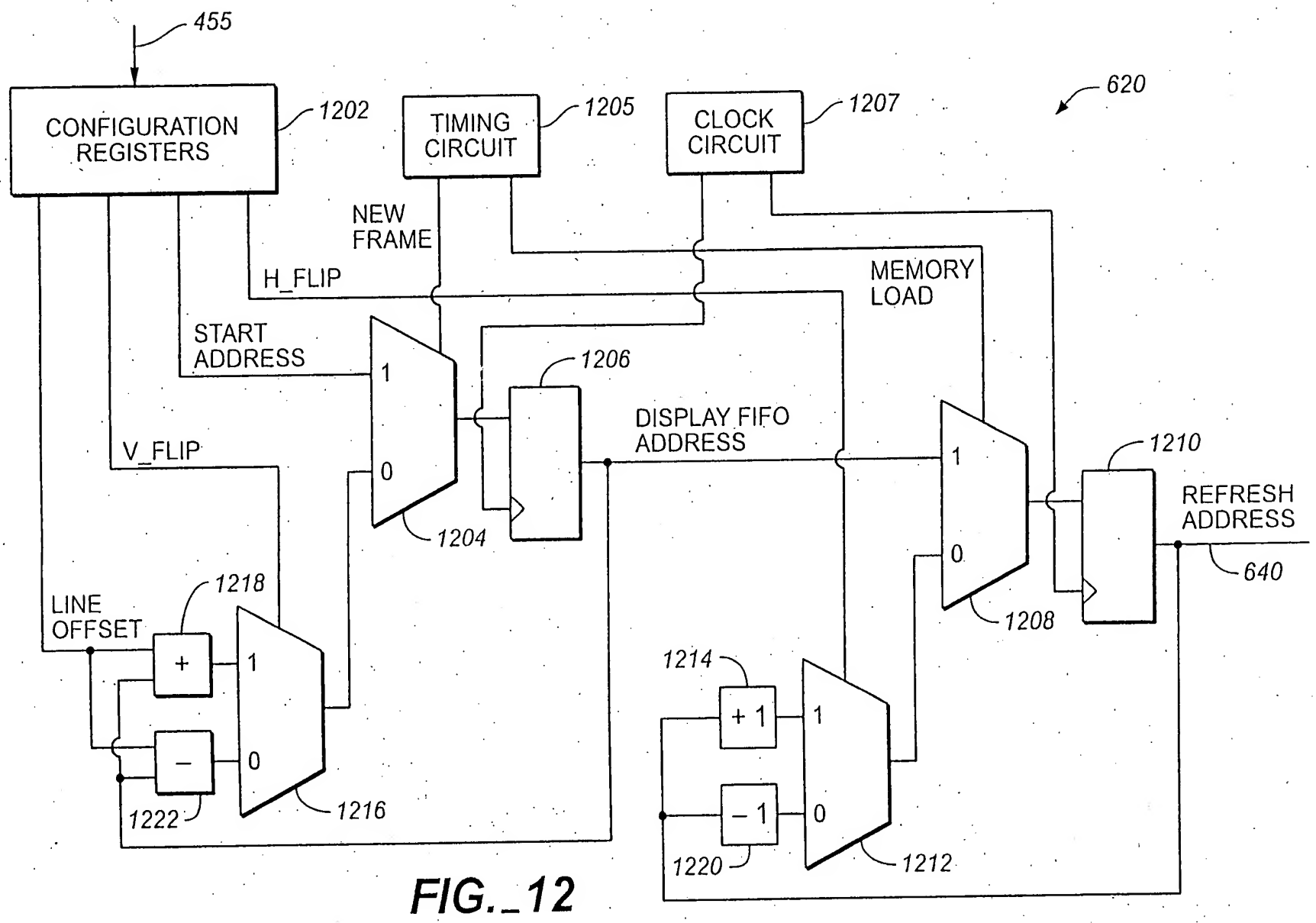
455
CONFIGURATION REGISTERS
1202
TIMING CIRCUIT
1205
CLOCK CIRCUIT
1207
620
NEW FRAME
H_FLIP
MEMORY LOAD
START ADDRESS
1
0
1204
1206
DISPLAY FIFO ADDRESS
V_FLIP
1
0
1208
1210
REFRESH ADDRESS
640
LINE OFFSET
1218
+
1
−
0
1222
1216
1214
+ 1
1
− 1
0
1220
1212

FIG._12

BEST AVAILABLE COPY

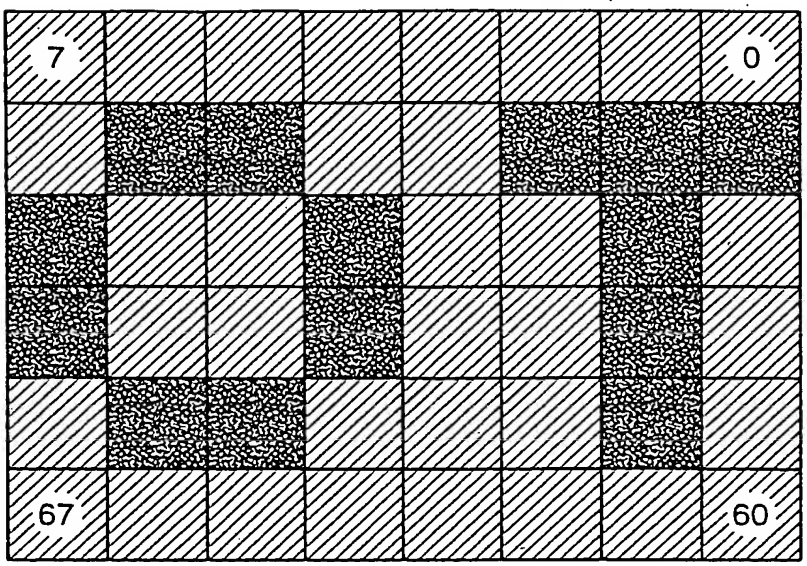

FIG._13

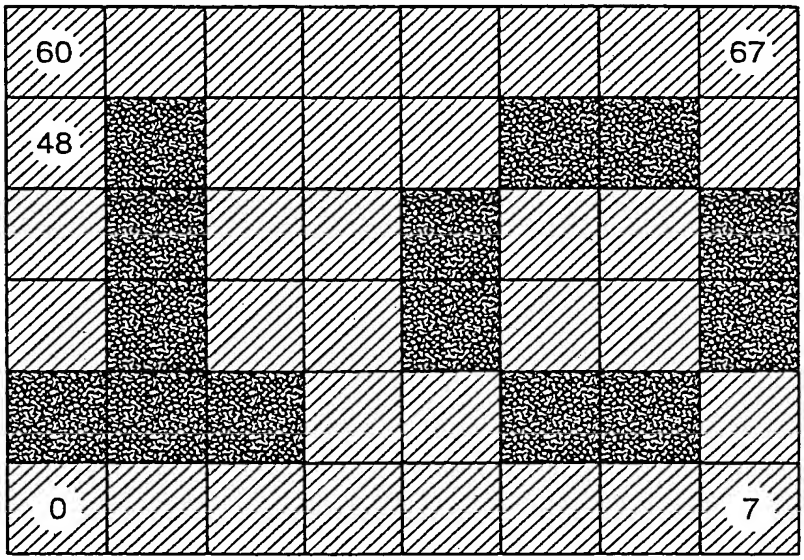

FIG._14

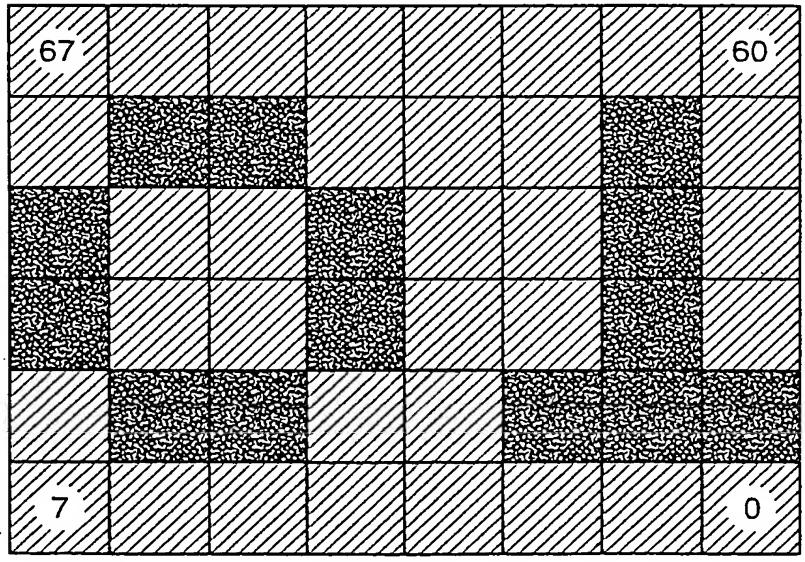

FIG._15